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Appl. No. : 10/659,374 Confirmation No. 3004

Applicant : K. SHIMADA

Filed : September 11, 2003

Title : A STORAGE SYSTEM AND A METHOD OF SPEEDING UP WRITING DATA INTO THE STORAGE SYSTEM

TC/AU : 2651

Examiner : TBD

Docket No. : H-1112

Customer No.: 24956

PETITION TO MAKE SPECIAL
UNDER 37 CFR §1.102(d) (MPEP §708.02(VIII))

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Applicants petition the Commissioner to make the above-identified application special in accordance with 37 CFR §1.102(d). In support of this Petition, pursuant to MPEP § 708.02(VIII), Applicants state the following.

(A) REQUIRED FEE

This Petition is accompanied by the fee set forth in 37 CFR § 1.117(h). A Credit Card Payment Form in the amount of \$130 accompanies this Petition in satisfaction of the fee. The Commissioner is hereby authorized to charge any

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additional payment due, or to credit any overpayment, to Deposit Account No. 50-1417.

(B) ALL CLAIMS ARE DIRECTED TO A SINGLE INVENTION

All the pending claims of the application, claims 1-15, are directed to a single invention. If the Office determines that all claims in the application are not directed to a single invention, Applicant will make election without traverse as a prerequisite to the grant of special status.

The claimed invention, as set forth in independent claims 1, 9, 10, and 15, is generally directed to a storage system and method in which the speed and reliability with which data is written from a host to a storage system is increased for a storage system with duplex cache memory. Under claim 1, the invention is a storage system that includes a storage device, a first controller, and a second controller, both connected to the storage device and a host system. The first controller has a first memory and a second memory, and the second controller has a third memory. In the case where the first controller receives data from the host system, the first controller stores the data in the first and second memories, and sends a response to the host system. Then, the first controller transfers the data stored in the second memory to the third memory.

Additionally, as set forth in claim 9, the invention is a storage system that includes a host interface unit connected to a host system, with a switching unit connected to the host interface unit. A first controller and a second controller are

connected to the switching unit, and a storage device is connected to the first and second controllers. The first controller has a first memory and a second memory, and the second controller has a third memory. In the case where the first controller receives data from the host system, the first controller stores the data in the first and second memory and sends a response to the host system, and then the first controller transfers the data stored in the second memory to the third memory.

Under further aspects, as set forth in claim 10, the invention is a storage system that includes a disk drive, a first cache memory for temporarily storing data sent from a host system so as to be written on the disk drive. Also included are a second cache memory for storing a duplicate of the data to be written on the disk drive, and a FIFO buffer for temporarily storing the duplicate of the data sent from the host system to transfer the duplicate of the data to the second cache memory. At the time when the data sent from the host system is stored in the first cache memory and the duplicate of the data sent from the host system is stored in the FIFO buffer, the host system is informed about the completion of data writing.

Additionally, as set forth in claim 15, the invention includes a method for writing data in a storage system having a duplex cache memory. The method includes writing data in one of the duplex cache memories for duplicating and storing data sent from a host system, and writing the data in a FIFO buffer capable of performing writing with a speed higher than that of the other one of the duplex cache memory. It is confirmed that the data has been correctly written in the one duplex cache memory and the FIFO buffer, and the host system is informed of the

completion of the data writing. The data written in the FIFO buffer is written in the other one of the duplex cache memories after the host system is informed about the completion of data writing to complete duplication of the data.

(C) PRE-EXAMINATION SEARCH

A careful and thorough pre-examination search has been conducted, directed to the invention as claimed. The pre-examination search was conducted in the following *US Manual of Classification* areas:

<u>Class</u>	<u>Subclass</u>
711	113, 114, 119, 120, 148, 162
714	5, 6, 14

Furthermore, a keyword search was conducted on the USPTO's EAST database. Additionally, a literature search was conducted for relevant non-patent documents using the Association for Computing Machinery online databases. In addition, a search for foreign patent documents was conducted on the European Patent Office's ESPACENET databases.

(D) DOCUMENTS DEVELOPED BY THE PRE-EXAMINATION SEARCH

Of the documents reviewed during the search, those deemed to be most closely related to the subject matter encompassed by the claims are listed below. These documents were made of record in the present application by the Information Disclosure Statement filed January 13, 2005.

Document No.

US 5708771

US 6438647

US 6681339

US 20040010658

US 20040153727

Inventor

Brant, William A. et al.

Nielson, Michael E. et al.

McKean, Brian D. et al.

Inoue, Yasuo

Hicken, Michael S. et al.

Additionally, the following documents were made of record in the present application by the Information Disclosure Statement filed November 11, 2003.

Document No.

JP09146842

JP2001318766

Inventor

Kobayashi, Rie et al.

Shiraishi, Kauya

Publication

IBM TotalStorage Enterprise Storage Server Model 800, IBM Redbooks, SG24-6424-01, 2ed., Oct. 2002, pp. 88-89.

Because all of the above-listed documents are already of record in the present application, in accordance with MPEP § 708.02(VIII)(D), additional copies of these documents have not been submitted with this Petition.

(E) DETAILED DISCUSSION OF THE REFERENCES

A discussion of each the above-listed documents is set forth below, pointing out, with the particularity required by 37 CFR 1.111 (b) and (c), how the claimed subject matter is patentable over the teachings of the above-listed documents.

The patent to Brant, US 5708771, shows a fault-tolerant controller system and method that includes at least two disk array controllers. A fast memory providing a buffer between a remote host computer and arrays of data storage media is managed so that data received for writing is duplicated for reliability of storage. A

failure of either of two primary power supplies causes the memory controller of the array controller, energized by the failed main output connection, to transfer data contained in its buffer memory into the buffer memory of the array controller energized by the main power output of the other of the power sources. (See, e.g., Abstract and column 3, lines 13-61.) Thus, Brant does not teach several aspects of the invention, including, in the case where a first controller receives data from a host system, the first controller stores the data in first and second memories, sends a response to the host system, and then the first controller transfers the data stored in the second memory to a third memory in a second controller, as set forth in claims 1 and 9. Nor does Brant teach that when data sent from a host system is stored in a first cache memory of a duplex, and a duplicate of the data is stored in a FIFO buffer from which the data will be stored to the second cache memory, the host system is informed about the completion of data writing, as set forth in claims 10 and 15. Accordingly, independent claims 1, 9, 10 and 15 are patentable over Brant.

The patent to Nielson, US 6438647, shows a write-back cache system in which, during normal operation, dual controllers operate in a write-back mode, which refers to the process of writing data in a receiving controller's cache and then writing data in the other controller's cache before returning a completion status to the host. Nielson's invention is directed to a dual controller write-back system with battery-backed data cache, wherein, when a controller fails, a replacement controller is installed, and the replacement controller needs to recondition its battery before the

write back cache mode is reinitiated. Under Nielson, battery state information is exchanged between controllers, and if any battery backup meets a predetermined threshold, all of the controllers run in write-back cache mode. (See, e.g., Abstract and column 2, line 46 – column 4, line 4.) Thus, Nielson does not teach the present invention, wherein a first controller receives data from a host system, the first controller stores the data in first and second memories, sends a response to the host system, and then the first controller transfers the data stored in the second memory to a third memory in a second controller, as set forth in claims 1 and 9. Nor does Nielson teach that when data sent from a host system is stored in a first cache memory of a duplex, and a duplicate of the data is stored in a FIFO buffer from which the data will be stored to the second cache memory, the host system is informed about the completion of data writing, as set forth in claims 10 and 15. Accordingly, independent claims 1, 9, 10 and 15 are patentable over Nielson.

The patent to McKean, US 6681339, shows a data storage system 100 utilizing a dual-active controller configuration. In accordance with a cache data mirror method, a Controller A (primary controller) 116 receives a write data request from the host system 102, wherein the write data request includes data to be written by the primary controller 116 to a storage subsystem. The primary controller 116 caches the data into the primary controller cache memory 120. Next, the primary controller 116 mirrors the data to Controller B (alternate controller) 118, such that the alternate controller 118 copies the data into an alternate controller cache memory

122, thereby providing a backup copy of the primary controller's 116 data in case of a controller failure. The cache memory in each controller includes a read/write (R/W) cache area, and a mirror area. The R/W cache area is used as an intermediate storage area for cache line data in order to provide the host system optimized access to the cache line data without having to access the storage subsystem. The mirror area is used to store a backup copy of cache line data mirrored from a partner controller. The mirror area is provided to allow a survivor controller to take over the tasks and cache line data of a failed controller. (See, e.g., Abstract and column 4, lines 26-63.) Thus, McKean does not teach the present invention, in which a first controller receives data from a host system, the first controller stores the data in first and second memories, sends a response to the host system, and then the first controller transfers the data stored in the second memory to a third memory in a second controller, as set forth in claims 1 and 9. Nor does McKean teach that when data sent from a host system is stored in a first cache memory of a duplex, and a duplicate of the data is stored in a FIFO buffer from which the data will be stored to the second cache memory, the host system is informed about the completion of data writing, as set forth in claims 10 and 15. Accordingly, independent claims 1, 9, 10 and 15 are patentable over McKean.

The published US patent application to Inoue, US 20040010658, shows an external storage subsystem having a plurality of independent cache units and nonvolatile memory units in a disk controller located between a host and a disk drive.

The cache units and the access paths to the cache units are multiplexed, so that a probability of maintaining cache function in case failure occurs is enhanced. Write data sent from the CPU 1 to the disk controller 2 is temporarily stored in one of the cache unit 80 and 81 and the nonvolatile memory unit 90 and 91 through the channel unit 60 or 61 and the one of the data buses 60A, 60B, 61A and 61B, in accordance with the command from the channel control processor 110 or 111. Then, the data is read from one of the cache units 80 and 81 or one of the nonvolatile memory units 90 and 91 by the command from the control unit control processor 120 or 121, and the write data is stored in the magnetic disk drive. (See, e.g., Abstract and paragraphs [0016] and [0042].) Thus, Inoue does not teach a system in which a first controller receives data from a host system, the first controller stores the data in first and second memories, sends a response to the host system, and then the first controller transfers the data stored in the second memory to a third memory in a second controller, as set forth in claims 1 and 9. Nor does Inoue teach that when data sent from a host system is stored in a first cache memory of a duplex, and a duplicate of the data is stored in a FIFO buffer from which the data will be stored to the second cache memory, the host system is informed about the completion of data writing, as set forth in claims 10 and 15. Accordingly, independent claims 1, 9, 10 and 15 are patentable over Inoue.

The published US patent application to Hicken, US 20040153727, shows a method for recovering cache data of a failed redundant storage controller and

reestablishing redundancy. The method includes arranging the storage controllers into pairs, such that cache data of the primary cache memory of each of the storage controllers in the pair is mirrored in the secondary cache memory of the other storage controller in the pair. (See, e.g., Abstract and paragraphs [0011]-[0012].) Hence, Hicken does not teach a system in which a first controller receives data from a host system, the first controller stores the data in first and second memories, sends a response to the host system, and then the first controller transfers the data stored in the second memory to a third memory in a second controller, as set forth in claims 1 and 9. Nor does Hicken teach that when data sent from a host system is stored in a first cache memory of a duplex, and a duplicate of the data is stored in a FIFO buffer from which the data will be stored to the second cache memory, the host system is informed about the completion of data writing, as set forth in claims 10 and 15. Accordingly, independent claims 1, 9, 10 and 15 are patentable over Hicken.

The Japanese patent publication to Kobayashi, JP9146842, discloses a technique of duplicating a cache memory of a storage system, and writing data in both of the cache memories for the purpose of reducing the probability of data loss, and improving reliability of the storage system. This storage system has the limitation of reducing response time because of the time consuming process of writing data in the duplex cache memory, and then reporting to the host system about the completion of writing. Since one of the control units serving to perform data transfer between the host system and the storage system transfers data to the

cache memory of the other control unit, and receives the report about completion of the data writing in the other control unit, it is necessary for the duplex control units to communicate with each other, and such communication is a main factor of prolonging the time required for the storage system to respond to the host system. (See, e.g., Abstract of Kobayashi and specification of the present application at pages 2-3.) Thus, Kobayashi does not teach the present invention, in which a first controller receives data from a host system, the first controller stores the data in first and second memories, sends a response to the host system, and then the first controller transfers the data stored in the second memory to a third memory in a second controller, as set forth in claims 1 and 9. Nor does Kobayashi teach that when data sent from a host system is stored in a first cache memory of a duplex, and a duplicate of the data is stored in a FIFO buffer from which the data will be stored to the second cache memory, the host system is informed about the completion of data writing, as set forth in claims 10 and 15. Accordingly, independent claims 1, 9, 10 and 15 are patentable over Kobayashi.

The Japanese patent publication to Shiraishi, JP2001318766, also discloses a technique of duplicating a cache memory of a storage system, and writing data in both of the cache memories for the purpose of reducing the probability of data loss, and improving reliability of the storage system. The disk array includes two controllers, and write data is executed in both controllers without using a shared memory. Thus, if a fault is generated in one of the controllers, the write data in the

other controller may be referred to. (See, e.g., Abstract of Shiraishi and specification of the present application at pages 2-3.) Thus, Shiraishi also does not teach the present invention, in which a first controller receives data from a host system, the first controller stores the data in first and second memories, sends a response to the host system, and then the first controller transfers the data stored in the second memory to a third memory in a second controller, as set forth in claims 1 and 9. Nor does Shiraishi teach that when data sent from a host system is stored in a first cache memory of a duplex, and a duplicate of the data is stored in a FIFO buffer from which the data will be stored to the second cache memory, the host system is informed about the completion of data writing, as set forth in claims 10 and 15. Accordingly, independent claims 1, 9, 10 and 15 are patentable over Shiraishi.

The IBM publication, *IBM TotalStorage Enterprise Storage Server Model 800*, discloses a technique of preventing data loss by the use of a non-volatile cache memory. Since the nonvolatile memory is provided in a control unit as a backup memory for a cache memory, the problem of delay due to data transfer between a duplex system does not occur. The data is written to the cache and written to the nonvolatile memory, and the host is notified that the I/O operation is complete as soon as the data is in the nonvolatile memory. However, unlike the present invention, the data is not then written from the nonvolatile memory to a second cache. (See, e.g., the IBM reference and discussion at pages 3-4 of the specification of present application.) Accordingly, the IBM reference does not teach the present

invention in which a first controller receives data from a host system, the first controller stores the data in first and second memories, sends a response to the host system, and then the first controller transfers the data stored in the second memory to a third memory in a second controller, as set forth in claims 1 and 9. Nor does the IBM reference teach that when data sent from a host system is stored in a first cache memory of a duplex, and a duplicate of the data is stored in a FIFO buffer from which the data will be stored to the second cache memory, the host system is informed about the completion of data writing, as set forth in claims 10 and 15. Accordingly, independent claims 1, 9, 10 and 15 are patentable over the IBM reference.

CONCLUSION

The Applicants submit that the foregoing discussion demonstrates the patentability of independent claims 1, 9, 10, and 15 over the closest-known prior art, taken either singly, or in combination. The remaining claims, claims 2-8 and 11-14, depend from claims 1 or 10, claim additional features of the invention, and are patentable at least because they depend from allowable base claims. Accordingly, the requirements of 37 CFR §1.102(d) having been satisfied, the Applicants request that this Petition to Make Special be granted and that the application be examined according to prescribed procedures set forth in MPEP §708.02 (VIII).

The Applicants prepared this Petition in order to satisfy the requirements of 37 C.F.R. §1.102(d) and MPEP §708.02 (VIII). The pre-examination search required by these sections was "directed to the invention as claimed in the application for which

special status is requested." MPEP §708.02 (VIII). The search performed in support of this Petition is believed to be in full compliance with the requirements of MPEP §708.02 (VIII); however, Applicants make no representation that the search covered every conceivable search area that might contain relevant prior art. It is always possible that prior art of greater relevance to the claims may exist. The Applicants urge the Examiner to conduct his or her own complete search of the prior art, and to thoroughly examine this application in view of the prior art cited above and any other prior art that may be located by the Examiner's independent search.

Further, while the Applicants have identified and discussed certain portions of each cited reference in order to satisfy the requirement for a "detailed discussion of the references, which discussion points out, with the particularity required by 37 C.F.R. §1.111(b) and (c), how the claimed subject matter is patentable over the references" (MPEP §708.02(VIII)), the Examiner should not limit review of these documents to the identified portions, but rather is urged to review and consider the entirety of each reference.

Respectfully submitted,



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